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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 07/27/2004

Birch Stewart Kolasch & Birch LLP
P O Box 747
Falls Church, VA 22040-0747

EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 07/27/2004

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/615,956	07/13/2000	Kumi Miyachi	1248-0509P	3629

TITLE OF INVENTION: SEMICONDUCTOR DEVICE HAVING INTEGRALLY SEALED INTEGRATED CIRCUIT CHIPS ARRANGED FOR IMPROVED TESTING

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1330	$0	$1330	10/27/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATEN PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHT THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPO PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM TH MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. TH STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOV REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (O AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WIL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is n claiming SMALL ENTITY status, check box 5a on Part B - Fee Transmittal and pay the PUBLICATION FEE (if required) and 1 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) w your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed wh appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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Birch Stewart Kolasch & Birch LLP
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I hereby certify that this Fee(s) Transmittal is being deposited with the Un States Postal Service with sufficient postage for first class mail in an envel addressed to the Mail Stop ISSUE FEE address above, or being facsim transmitted to the USPTO (703) 746-4000, on the date indicated below.

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(Signat
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nonprovisional	NO	$1330	$0	$1330	10/27/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
ABRAHAM, ESAW T	2133	714-724000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent); ❑ individual ❑ corporation or other private group entity ❑ governm

4a. The following fee(s) are enclosed:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s):

❑ A check in the amount of the fee(s) is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is not claiming SMALL ENTITY status. See, e.g., 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other part interest as shown by the records of the United States Patent and Trademark Office.

(Authorized Signature) (Date)

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to proc an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to comp this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 14 Alexandria, Virginia 22313-1450.

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2133	

DATE MAILED: 07/27/2004

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 317 day(s). If the issue fee is paid on the date that is three months after t mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a ha months) after the mailing date of this notice, the Patent Term Adjustment will be 317 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date th determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retriev (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Notice of Allowability	Application No.	Applicant(s)	
	09/615,956	MIYACHI ET AL.	
	Examiner	Art Unit	
	Esaw T Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/26/04*.

2. ☒ The allowed claim(s) is/are *2-4,6,7,9,11 and 13-16 (renumbered as 1-12)*.

3. ☒ The drawings filed on *27 November 2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

Examiner's statement for reason for allowance

The following is an examiner's statement for allowance:

1. Amended claim 13 is accepted by the examiner.

2. Claims **2-4, 6, 7, 9-11 and 13-16** have been allowed.

As per claim **2,** the prior art (Brown et al. (U.S. PN: 5,627,842)) of record teach Brown et al. disclose a semiconductor device comprising plurality of chips (see figure 2 and col. 3, lines 49-55), a test signal input terminal for receiving a test signal (see fig. 2, edge connector coupled to the input TDI and col. 4, lines 3-9), a test output terminal for outputting a test result of plurality of chips to outside (see fig. 2, edge connector coupled to the output TDO), a control signal input terminals for receiving a test control signals (see fig. 2, edge connector coupled to the inputs TMS and TCK) whereby the test signal inputted transferred through the plurality of chips (see fig. 2, "input TDI" and col. 4, lines 3-27). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a test control signals inputted from said control signal input terminals being individually supplied to each of the said plurality of chips wherein said plurality of chips are connected to each other via said test result output terminal. Consequently, claim 2 is allowed over the prior art.

Claim **15,** which is directly or indirectly dependent of claim 2, is also allowable over the prior art of record.

As per claim **3,** the prior art (Brown et al. (U.S. PN: 5,627,842)) of record disclose a semiconductor device comprising plurality of chips (see figure 2 and col. 3, lines 49-55), a test signal input terminal for receiving a test signal (see fig. 2, "input TDI" and col. 4, lines 3-9), a

test output terminal for outputting a test result of plurality of chips to outside (see fig. 2, "output TDO"), a control signal input terminals for receiving a test control signals (see fig. 2, inputs TMS and TCK). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a test signal being inputted to one of said plurality of chips and successively transferred through the other chips, and after being inputted again into the one of said plurality of chips, outputted as the test result outside and the test control signal being individually supplied from one of said plurality of chips to each of the other chips. Consequently, claim 3 is allowed over the prior art.

Claims **4 and 16,** which are directly or indirectly dependents of claim 3 are also allowable over the prior art of record.

As per claim **6,** the prior art (Brown et al. (U.S. PN: 5,627,842)) of record disclose a semiconductor device comprising plurality of chips (see fig. 2), a test registers providing between core logic and the chips (see fig. 2, "the small squares surrounded the core logic" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4, lines 28-63), a test data input (see fig. 2, edge connector coupled to the input of TDI), a test data output (see fig. 2, edge connector coupled to the output of TDO). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a test/command data output terminal of a chip being connected to a corresponding output terminal of a device and serially to the test/command data input terminal of a chip of a following stage via the output terminal of the device. Consequently, claim 6 is allowed over the prior art.

As in claim 7, the prior art (Brown et al. (U.S. PN: 5,627,842)) of record disclose a semiconductor device comprising plurality of chips, a test data input connected to the test data

input of a first stage (see fig. 2, input of the line TDI) and serially connected to the test data input of a chip of a following stage (see fig. 2, "the lines that connect the four IC's and col. 4, lines 3-27), a test registers providing between core logic and the chips (see fig. 2, "the small squares surrounded the core logic" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4, lines 28-63), a test data input (see fig. 2, edge connector coupled to the input of TDI) and test data output (see fig. 2, edge connector coupled to the output of TDO). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a relay output terminal of the chip of the first stage being connected to a test command/data input terminal of a chip of the following stage and a test command/data output terminal being serially and successively connected between chips of a preceding stage and a following stage and a test command/data output terminal of a chip of the last stage being connected to the relay input terminal of the chip of the first stage as to form a loop and the output terminals of the chip of the first stage for the signals to be used in the test being connected to input terminals of the signals of the other chips. Consequently, claim 7 is allowed over the prior art.

As per claim **9,** the prior art (Brown et al. (U.S. PN: 5,627,842)) of record disclose a semiconductor device comprising plurality of chips (see figure 2 and col. 3, lines 49-55), a test signal input terminal for receiving a test signal (see fig. 2, edge connector coupled to the input TDI and col. 4, lines 3-9), a test output terminal for outputting a test result of plurality of chips to outside (see fig. 2, edge connector coupled to the output TDO), a control signal input terminals for receiving a test control signals (see fig. 2, edge connector coupled to the inputs TMS and TCK) whereby the test signal inputted transferred through the plurality of chips (see fig. 2,

"input TDI" and col. 4, lines 3-27). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a test control signals inputted from said control signal input pins being individually supplied to each of the said plurality of chips wherein said plurality of chips are connected to each other via said test result output pin. Consequently, claim 9 is allowed over the prior art.

As per claim **10,** the prior art (Brown et al. (U.S. PN: 5,627,842)) of record disclose a semiconductor device comprising plurality of chips (see figure 2 and col. 3, lines 49-55), a test signal input terminal for receiving a test signal (see fig. 2, "input TDI" and col. 4, lines 3-9), a test output terminal for outputting a test result of plurality of chips to outside (see fig. 2, "output TDO"), a control signal input terminals for receiving a test control signals (see fig. 2, inputs TMS and TCK). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a test signal being inputted to one of said plurality of chips and successively transferred through the other chips, and after being inputted again into the one of said plurality of chips, outputted as the test result outside and the test control signal being individually supplied from one of said plurality of chips to each of the other chips. Consequently, claim 10 is allowed over the prior art.

Claim **11,** which is directly or indirectly dependent of claim 10, is also allowable over the prior art of record.

As per claim **13,** the prior art (Brown et al. (U.S. PN: 5,627,842)) of record disclose a semiconductor device comprising plurality of chips, a test registers providing between core logic and the chips (see fig. 2, "the small squares surrounded the core logic" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4,

lines 28-63), a test data input (see fig. 2, edge connector coupled to the input of TDI), a test data output (see fig. 2, edge connector coupled to the output of TDO). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a test/command data output terminal of a chip being connected to a corresponding output pad of a device and serially to the test/command data input pin of a chip of a following stage via the output pins of the device. Consequently, claim 13 is allowed over the prior art.

As in claim **14,** the prior art (Brown et al. (U.S. PN: 5,627,842)) of record disclose a semiconductor device comprising plurality of chips, a test data input connected to the test data input of a first stage (see fig. 2, input of the line TDI) and serially connected to the test data input of a chip of a following stage (see fig. 2, "the lines that connect the four IC's and col. 4, lines 3-27), a test registers providing between core logic and the chips (see fig. 2, "the small squares surrounded the core logic" in each of the chips), a controller (TAP controller) for controlling the test registers and for testing the chip (see col. 4, lines 28-63), a test data input (see fig. 2, edge connector coupled to the input of TDI) and test data output (see fig. 2, edge connector coupled to the output of TDO). However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a relay output pad of the chip of the first stage being connected to a test command/data input pad of a chip of the following stage and a test command/data output pad being serially and successively connected between chips of a preceding stage and a following stage and a test command/data output pad of a chip of the last stage being connected to the relay input pad of the chip of the first stage as to form a loop and the output pad of the chip of the first stage for the signals to be used in the test being connected

to input pads of the signals of the other chips. Consequently, claim 14 is allowed over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2